

JEDEC STANDARD

Test Methods to Characterize Voiding in Pre-SMT Ball Grid Array Packages

JESD217A.01

(Revision of JESD217.01, October 2016)

NOVEMBER 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES

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Forward

This document has been prepared by the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices.

Introduction

As ball grid array device pitch continues to decrease, the need to characterize solder voiding has become more significant. Solder void manifestation (type and/or sizes) has been used to determine process capability as a means of quality assurance during process transfer, and as indicators of process stability from in-line manufacturing monitors. This document describes how to characterize voids in solder spheres in ball grid array packages prior to surface-mount (SMT) reflow soldering.

TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES

(From Board Ballot JCB-22-35, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This standard provides an overview of solder void types, outlines current metrologies and test methods used for pre-SMPT solder void characterization and potential limitations, and prescribes sampling strategy for data collection, and tolerance guidelines for corrective measures.

Test methods can be applied to several types of ball grid array packages such as FCBGA, PBGA, CBGA, and CCGA with minimum 0.5 mm ball-to-ball pitch and constructed with leaded and lead-free solder alloys.

Guidelines for pre-SMT voids may not be sufficiently robust where ball grid array packages balls are assembled onto unfilled micro-via structures on package substrate land. Hence, the un-filled microvia construction (Figure 1 (a)) is considered out-of-scope for this document, while filled via (Figure 1 (b)) is within scope.

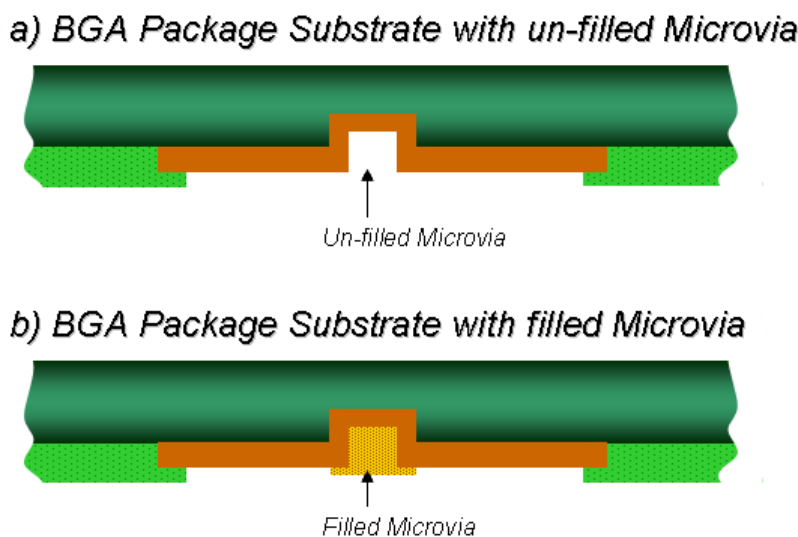


Figure 1 — Illustration of Unfilled Microvia (a) Out-of-Scope vs. Filled Microvia (b) In-Scope of Document

2 Terms and Definitions

ball grid array (BGA) packages: A package in which the external connections to the package are made via a rectangular array of ball-type connections, all on a common plane. (Ref. definition per JESD22-B112.)

CBGA: Ceramic ball grid array package.

CCGA: Ceramic column grid array package.

field of view: The area of the test sample under metrology examination.

flip chip ball grid array (FCBGA) package: A type of ball grid array (BGA) package which consists of facedown die (flip chip FC) on organic substrate of package.

NOTE FCBGA packages typically have a filled epoxy which is dispensed between the die and the substrate.

lead solder: A solder sphere composed primarily of tin (Sn) and lead (Pb) elements.

NOTE 67%/37% (SnPb) and 60%/40% (SnPb) are predominant formulations, and are commonly referred to as eutectic solder.

Pb-free; lead-free: Having a maximum lead (Pb) concentration value of 0.1% by weight in PCB surface finishes, device terminal finishes, bump or ball materials, and attachment solders.

NOTE Pb-free SAC alloys: traditional tin/silver/copper alloys that have a melting point in the range of 217°C and 220°C.

NOTE LTS (Low Temperature Solder) alloys: near eutectic-bismuth alloys that have a melting point in the range of 150°C and 170°C.

PBGA: Plastic ball grid array package.

Printed Circuit Board (PCB): Printed board that provides both point-to-point connections and printed components in a predetermined arrangement on a common base (also sometimes termed Printed Wiring Board). (Ref. IPC-T-50G)

SAC: A type of lead-free solder made from tin, silver, and copper (Sn=S, Ag=A, Cu=C). (Ref. IPC-7095B)

surface mount process technology (SMT): A method of constructing electronic printed circuit boards in which components (small or large devices) are placed onto solder paste (or flux) in specified locations and exposed to reflow process window with varying sets of elevated temperature and time that allows solder coalescence and metallization.

solder void area: The area of the solder void region within the X-ray image of a BGA solder ball or joint.

3 Normative References

J-STD-609, *Marking, Symbols, and Labels of Leaded and Lead-Free Terminal Finished Materials Used in Electronic Assembly*

JESD16-A, *Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM)*

JESD47, *Stress-Test-Driven Qualification of Integrated Circuits*

JESD22-B112, *Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperature*

IPC-A-610D, *Acceptability of Printed Circuit Assemblies*

IPC-7095B, *Design and Assembly Process Implementation for BGAs*

IPC-T-50G, *Terms and Definition for Interconnecting and Packaging Electronic Circuits*

4 Ball Attach Process Flow

Solder balls are attached by applying a flux/paste material on to the BGA pads, placing the solder balls on the pads, and reflowing the BGA package. The reflow process forms a metallurgical joint between the solder ball and the substrate ball pad. Alignment is a key parameter during ball placement to avoid missing solder balls or solder balls bridging.

Figure 2 gives a sequential representation of the BGA ball attach process flow.

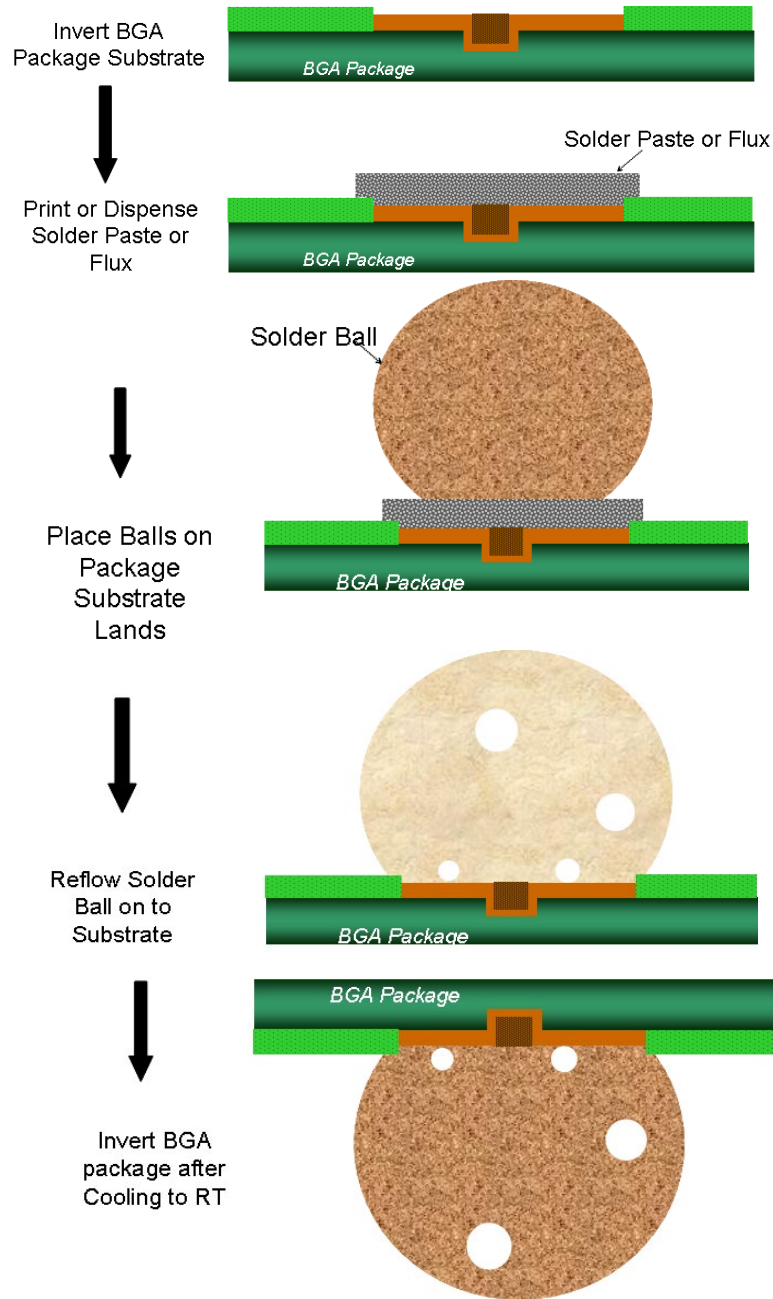


Figure 2 — BGA Ball Attach Process Flow Diagram

5 Types of Solder Voids

For the sake of completeness, all six types of voids observed in solder joints are described in this section, including potential voids that manifest after BGA-type packages are mounted onto a board. The individual characteristics of each of these voids are detailed here.

Macrovoids are the most common voids in solder joints. These are caused by volatile compounds that evolve during the soldering processes. These macrovoids generally do not affect the solder joint reliability unless they are present at interfacial regions in the solder joints where cracks typically propagate. This type of voids is within scope of this document.

Planar Microvoids are a series of small voids, in relatively the same plane, located at the interface between the PCB lands and the solder. These are caused by copper caves predominantly observed under immersion silver (ImAg) surface-finish coated lands. They do not affect initial product quality, but can affect long term solder joint reliability. They can be eliminated by strict control of the ImAg surface finish plating and etching materials and critical process parameters.

Shrinkage Voids are caused by the shrinkage during solidification, mostly for SAC and other lead free solders. They do not generally appear near the solder-to-PCB land interface and do not impair the solder joint reliability. These shrinkage voids can be minimized by increasing the cooling rate during soldering and avoiding disturbance to the joint while it is solidifying.

Micro-via Voids are caused by the presence of micro-vias designed in the PCB lands. Large micro-via voids, if located in solder joints in high stress areas of a package can impact solder joint reliability. Plating the micro-via shut, or filling it completely with solder paste by double printing can minimize the creation of these voids.

IMC Microvoids occur within the intermetallic compound (IMC) formed between copper and high Sn solders, including SAC and SnPb solders. These IMC microvoids do not form immediately after the soldering process, but after aging at high temperatures or during temperature cycling of the solder joints. The true root cause is still under investigation, but a *Kirkendall* voiding mechanism may play a part. These voids can affect solder joint reliability, particularly in instances when brittle fracture is initiated within the IMC during drop or mechanical shock to the solder joint.

Pinhole Voids are caused by pinholes in the copper lands of the PCB. With sufficient quantity, they can affect solder joint reliability. These voids are caused by entrapped PCB fabrication chemicals within these pinholes that volatilize during the reflow soldering process. The pinholes occur due to an excursion within the copper plating process at the PCB fabricator and can be eliminated by improved copper plating process control systems. These types of voids are considered out-of-scope

5 Types of Solder Voids (cont'd)

Figure 3 illustrates all six types of voids and their typical size and location in a BGA solder joint.

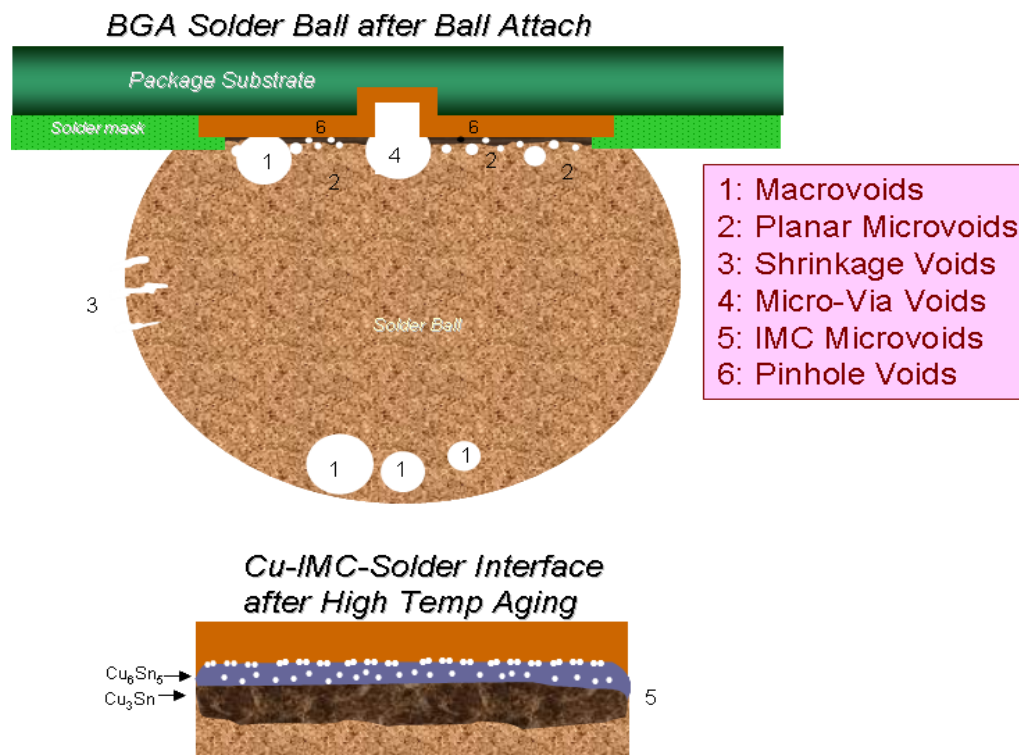


Figure 3 — Typical Size and Location of Various Types of Voids in a BGA Solder Joint

For this standard, focus is placed on macrovoids, because they are most likely to manifest prior to SMT process and can be identified by most metrologies. The other types of voids are noted for completeness, but out-of-scope due to metrology detection and void formation concerns.

6 Solder Void Metrologies

6.1 2-D X-ray

2-D X-ray is one of the metrologies being used to detect and measure the voids in BGA solder joints. There are a variety of 2-D X-ray tool vendors. Care must be taken to optimize the tool settings to achieve the best possible measurements. Generic guidelines for the 2-D X-ray technique are described in this section.

6.1.1 2-D X-Ray Tool Requirement/Limitation

The X-ray tube should be perpendicular to the test sample during image capture, as shown in Figure 4. Oblique viewing does not provide “true” void %.

The field of view may be modulated by adjusting the distance between the test sample and X-ray tube. Field of view ought to be set considering accuracy of the inspection as well as throughput requirements. Variations in the field of view that permits 3x3, 4x4 and 5x5 ball array are commonly reported.

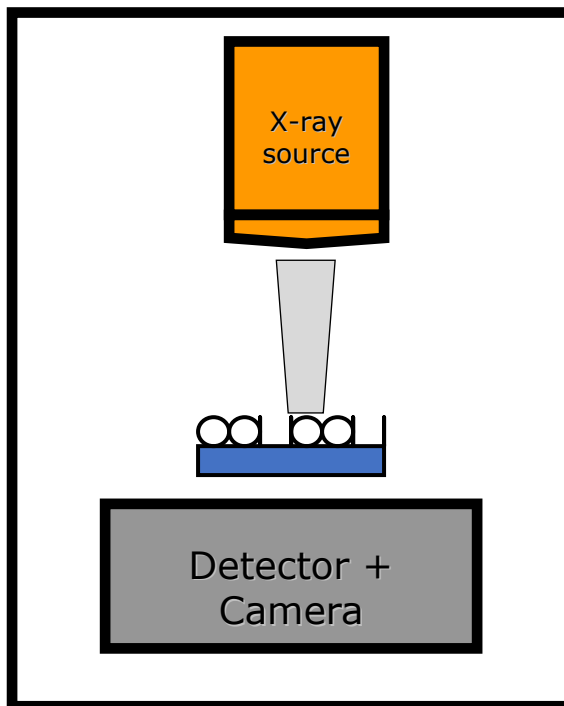


Figure 4 — Illustration of X-ray Setup and its Orthogonal Alignment to Test Sample

To achieve the best possible contrast between BGA voids and the surrounding area for solder void detection, adjustments to the grey scale should be considered. Ranges of settings that may be utilized as starting points are provided. The settings are given in terms of % grey scale (black is 0%, white is 100%):

- Solderball setting range from 36% to 48%.
- Background setting range from 85% to 100%.

The above settings can be achieved by adjusting the current and voltage on the X-ray tool. Figure 5 emphasizes the importance of proper contrast; voids are barely visible in the left image, while the right image was collected after achieving the best possible contrast.

6.1.1 2-D X-Ray Tool Requirement/Limitation (cont'd)

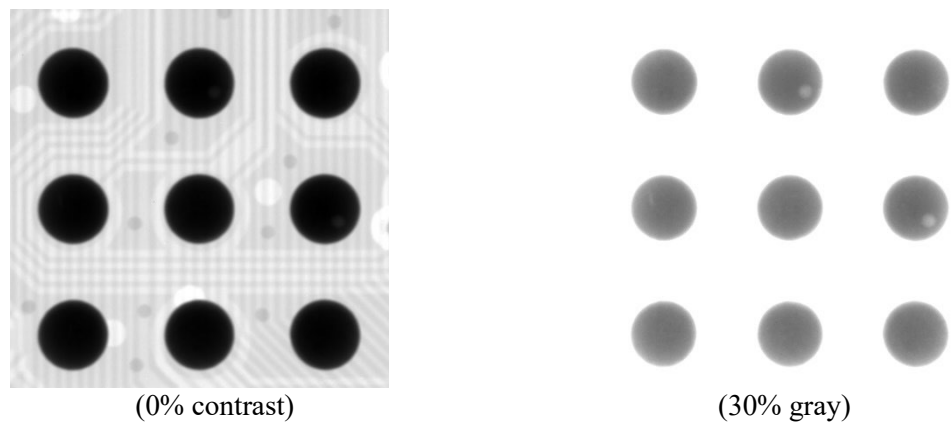


Figure 5 — Example of Contrasting in Grey Scaling (0% to 30% Gray) Permitting Detection of Solder Voids

In general, 2-D X-ray metrology provides some advantages such as general availability, ease of operation, non-destructive nature to test samples, and faster throughput over other techniques like 3-D X-ray and cross-section. However, it has some limitations which are given in Table 1.

Table 1 — 2-D X-ray – Potential limitations

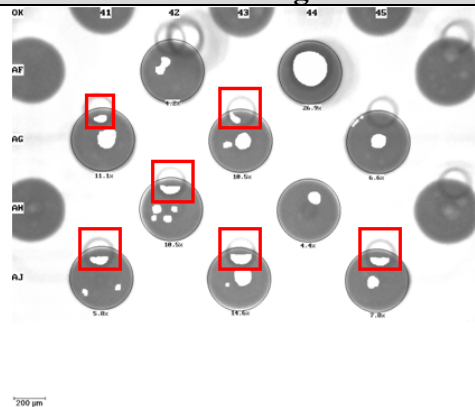
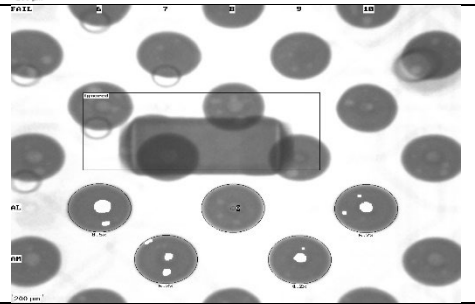
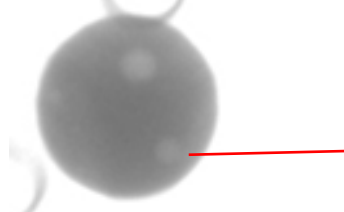
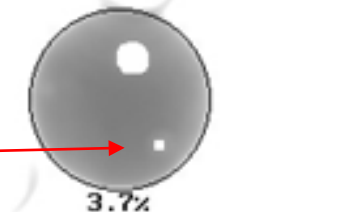
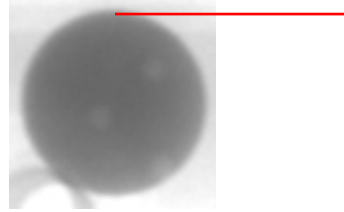
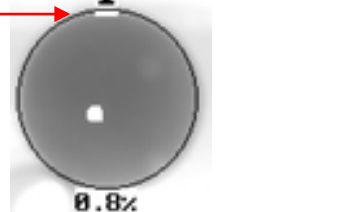
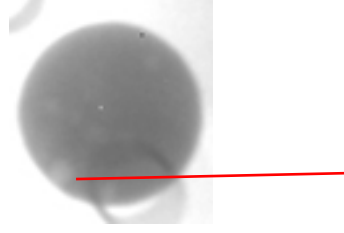
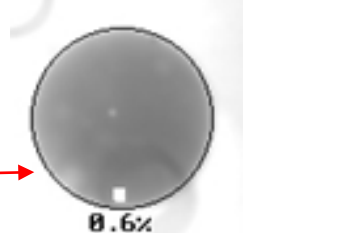
Item	Image
Plated Thru Hole via interference. The red squares in the image at the right indicate where the software algorithm for automatic void calculation has incorrectly identified via hole outlines that intersect the BGA ball outline as solder voids. This results in an over-estimation of the cumulative % void area within the BGA ball from the X-ray image.	
Interference of passive devices (like capacitors) with BGA solder joints. The software algorithm for automatic void calculation did not identify and measure the voids in the solder ball images that intersect the chip capacitor image within the figure at the right.	

Table 1 — 2-D X-ray – Potential limitations (cont'd)

Item	Image Before Measurement	Image After Measurement
The entire void area is not being measured by the automated software algorithm.		 3.7%
Edge areas in the solder ball image are incorrectly being measured as voids in the ball image.		 0.8%
Voids in the edge areas of the solder ball image are being missed during measurement by the automated software algorithm.		 0.6%

Some of the limitations can be attributed to software algorithms provided with the tools, while others are dependent on the type and location of solder voids or inherent to 2-D transmission X-ray technology itself. Nevertheless, 2-D X-ray metrology can be used in conjunction with stand-alone image analysis software applications.

6.2 3-D Computer Tomography X-ray

3-D- X-ray tomography can be used as an engineering tool to image, measure and locate solder joint voids. Tomography imaging involves three main steps:

- 1) Image acquisition (collect shadow images as the sample rotates through at least 180 degrees).
- 2) Software reconstruction that renders the 3-D volume.
- 3) Inspection where the size, shape, location and dimensions of the solder joint may be established and measured.

6.2 3-D Computer Tomography X-ray (cont'd)

Figure 6 shows the progressive nature of the 3-D X-ray scanning process to capture the void and void diameter determination.

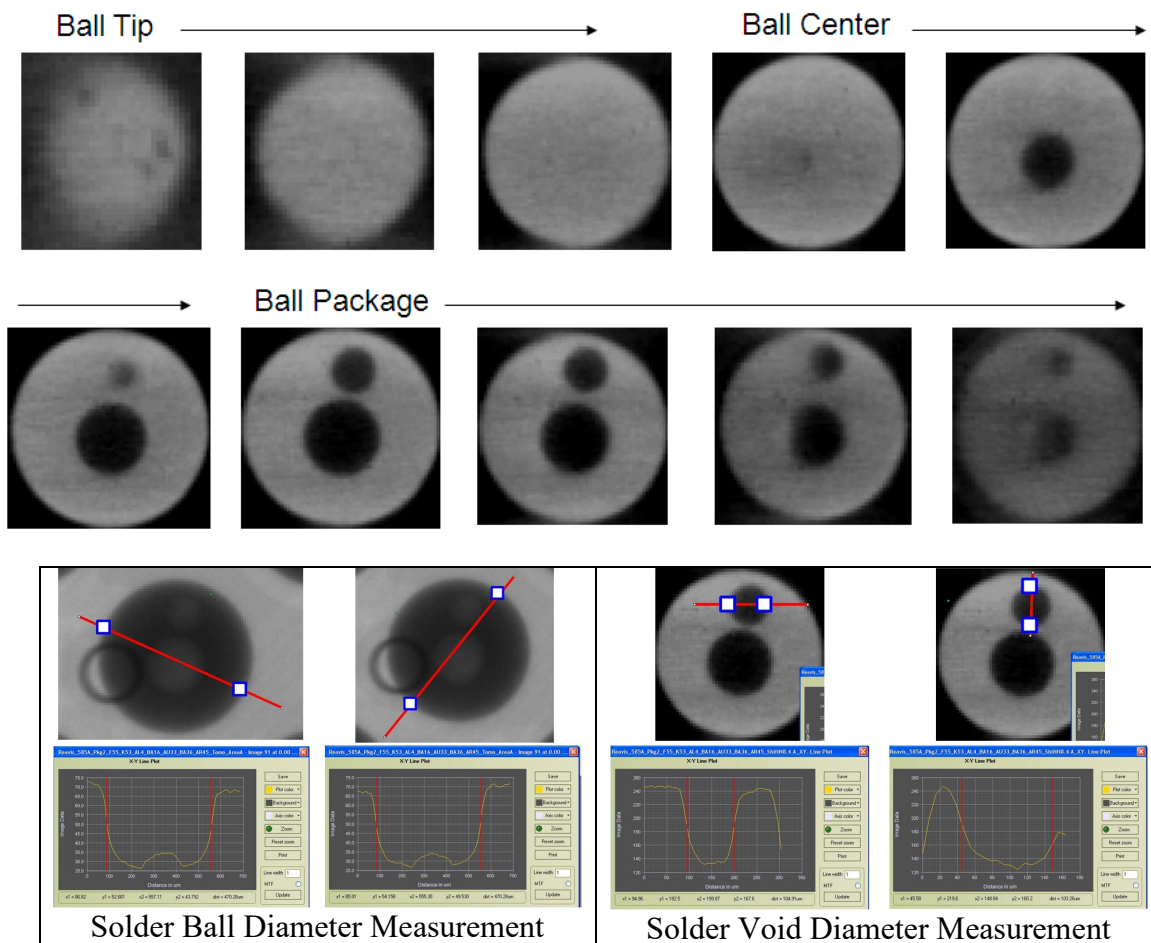


Figure 6 — Illustration of the 3-D X-ray Scanning Process and Void Diameter Computation

6.2.1 3-D CT X-Ray Tool Requirement/Limitation

For true 3-D tomography, the sample-detector and sample-source distances should be chosen such that the sample being imaged can rotate freely over an entire arc of 180 degrees without colliding with either the X-ray source or detector. This limits the size of the sample that can be accommodated by the instrument.

Another limitation is the amount of time required for data collection and analysis. While the 3-D X-ray method overcomes most of the limitations of 2-D transmission techniques, long throughput time and sample size constraints exclude tomography as a high volume choice for solder joint void assessment.

6.3 BGA Void Measurement Using 5DX Laminography

Laminography in the context of the 5DX is the process of focusing on a plane in a solder joint (slice height). From above the X-ray target, the electron beam is synchronized at 180 degrees following the rotary scintillator, positioned below the board being tested.

6.3.1 Image Acquisition Setup

In Figure 7, **A** is in the image (focal) plane, while **B** is outside. Note that **A** always projects to the same location on the scintillator screen, while **B** projects to constantly changing locations. As a rotation of the scintillator is completed, the **B** image averages out of the view, leaving only **A**. The laminography image, referred to as a slice, (**A**) projects onto the scintillator screen where it is converted to normal light for the X-ray image camera. Mirrors within the rotatory scintillator act as a periscope to transfer the image to the fixed position X-ray image camera. The X-ray image camera sees the slice as a real-time image of the cross-section at the plane of focus.

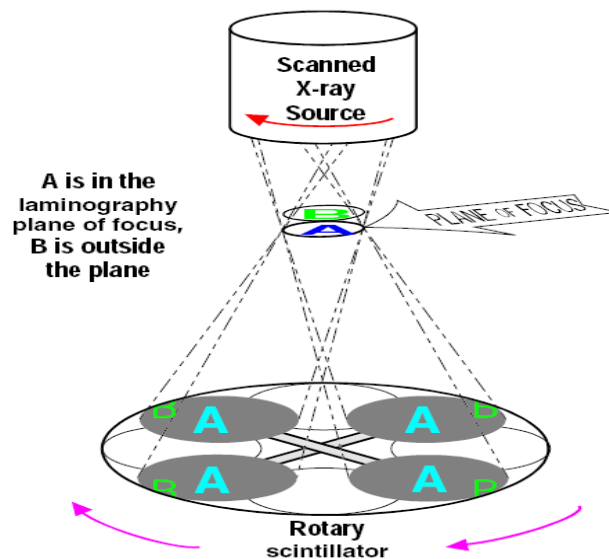


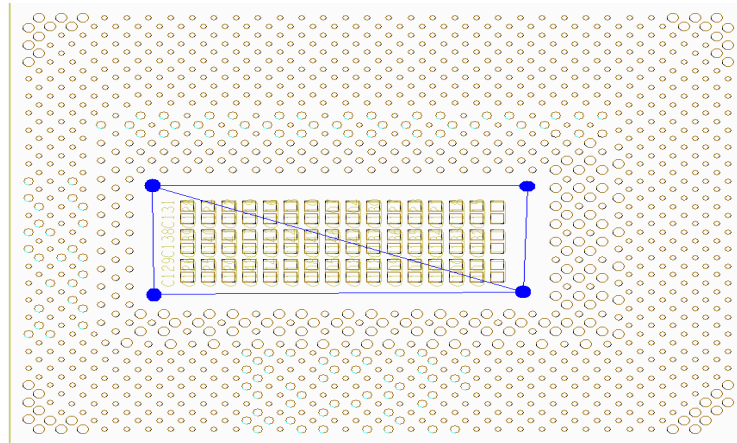
Figure 7 — Schematic Diagram of a 5DX X-ray Laminography Tool

6.3.2 Surface Mapping to Compensate for Warpage

To ensure that the focal plane is located at the correct height the system needs to surface map the device to compensate for warpage. This can be challenging as you need a plane that is long enough in the X direction to completely contain the laser. Ideally these points would be near the corners of the device, but you cannot always place them there due to the solder balls being in the way.

6.3.2 Surface Mapping to Compensate for Warpage (cont'd)

The system calculates the Z-height for the XYZ Stage for each view by using the three points that form the triangle for that view. It assumes that within each triangle the board is usually tilted with at least a flat (not a curved) surface. It constructs a plane based on the X, Y locations and the Z-heights measured during the surface map. It calculates where the center of the view is in relation to the three points on that plane and what Z-height should be used. Figure 8 illustrates a surface map location on the bottom side of the package substrate.



NOTE Blue dots signify surface map points.

Figure 8 — Surface Map Location on the Bottom Side of the Package Substrate

5DX testing of packages will require using carriers to support the device. See example of one such carrier in Figure 9. Carriers are designed to locate devices in the lower left corner in relation to the direction the carrier is loaded into the tester.

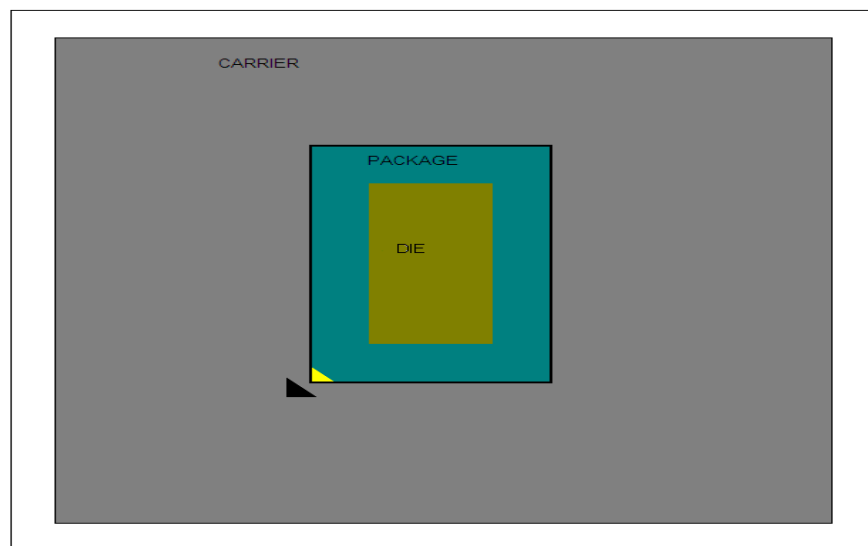


Figure 9 — Example of a Carrier Used to Support the Test Sample During 5DX Laminography Measurements

6.3.3 Setting Slice Heights

Slice 1 or center slice should be located at the center of the ball and should be determined by viewing the image on the 5DX. The top slice should be placed at 2x of the center slice. Finally the bottom slice should be placed near the bottom of the ball. For post SMT testing the bottom slice would be placed at the SMT pad. It is important to note that voids can be located in between the slices and therefore an accurate measurement will not be made. Figure 10 illustrates the instrumental limitation.

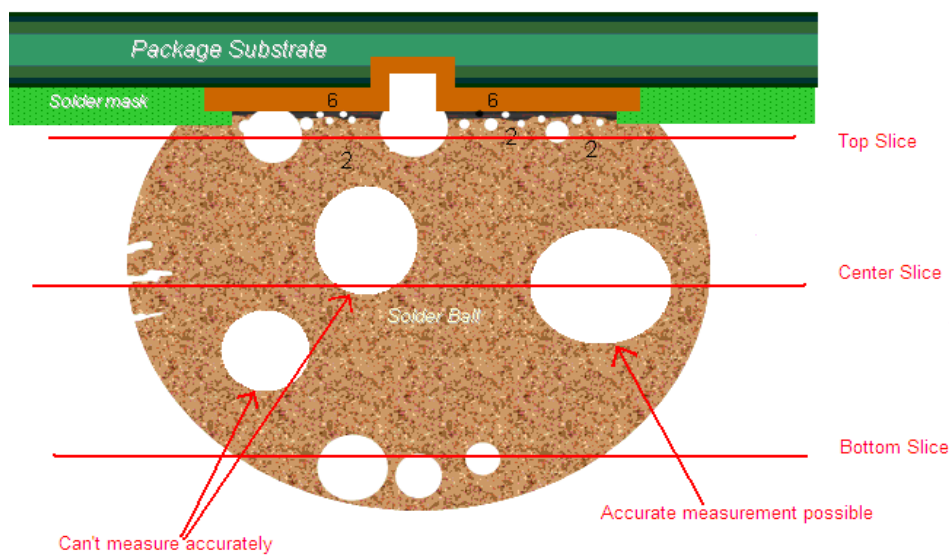


Figure 10 — Approximate Location of Three Slices for a BGA Ball Across Which the Cumulative % Void Area is Determined by the 5DX Laminography Tool

6.3.4 Voiding Algorithm Setup

After slice heights have been set so that good images are in focus, the operator must set the BGA voiding algorithm as specified by the vendor. Sensitivity and other parameters will need to be adjusted on a case by case basis, as these parameters will be set based upon the package design.

To determine proper algorithm settings the programmer can use the diagnostic utility. In diagnostics all pixels with a lighter gray scale than the threshold set will turn yellow to show the programmer how well the set thresholds captured the void size. Sensitivity settings determine what gray scale is considered void area.

Percent void is calculated by dividing the number of pixels that are below the threshold, by the number of pixels above, as shown in Figure 11.

6.3.4 Voiding Algorithm Setup (cont'd)

Note that the percent void is calculated for a given slice and therefore the region size for the top and bottom slices will be smaller than the true ball diameter (center slice), due to the spherical shape of the ball, as shown in Figure 11.

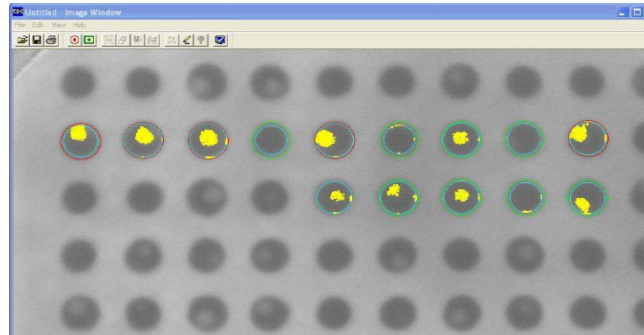


Figure 11 — Example of an Image of 5DX Laminography Tool Which Shows the Solder Balls and the Voids Within Them (Yellow)

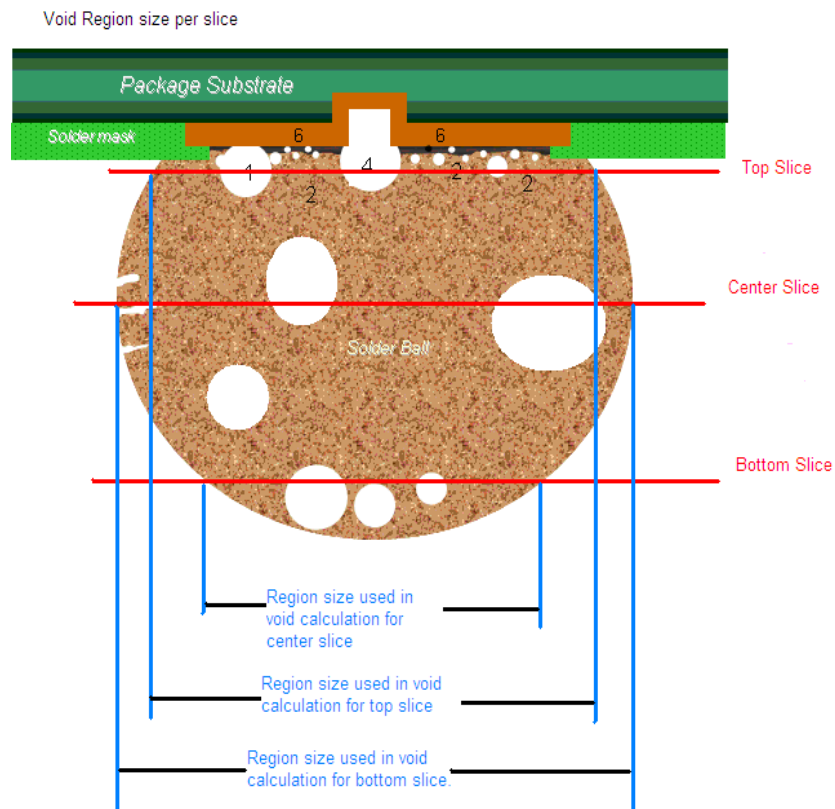


Figure 12 — Example of Region Size Per Slice

6.3.4 Voiding Algorithm Setup (cont'd)

While 5DX is fully automated with very good throughput time, it possesses many limitations. Primarily, 5DX is normally used as binary metrology (pass/fail) because of lack of accuracy. 5DX data is subjected to sensitivity and region settings. It is not robust to test samples with multiple voids in the same solder ball. Finally, small voids may be dismissed if they fall between slices (see Figure 12). Moreover, 5DX is not particularly suitable for package testing due to alignment issues (no clear fiducials) and challenges with inherent package warpage.

6.3.5 Cross Section

Metallographic cross-sectioning is one of the conventional destructive metrologies to detect and measure the voids in BGA solder joints. Generic guidelines about this technique are described in IPC 2.1.1E. Though it gives the ability to measure the true size of the void; some of the challenges are:

- 1) Location of voids in the solder joint requires repeated careful sectioning of the sample. The sequence of the grinding and polishing steps is shown diagrammatically in Figure 13.

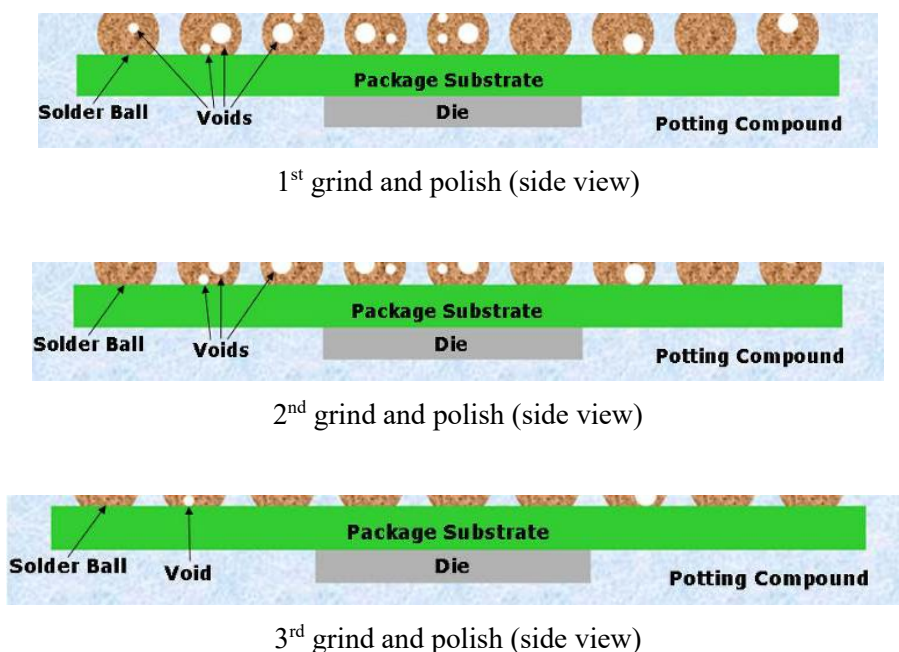
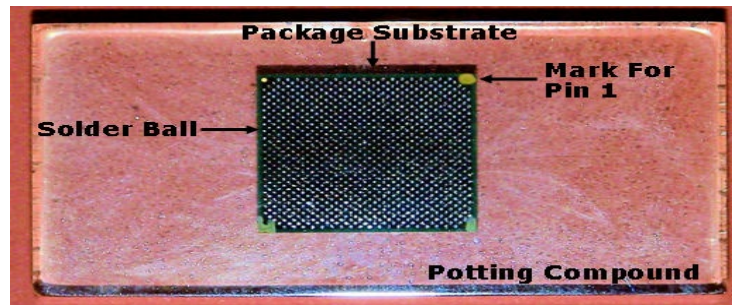


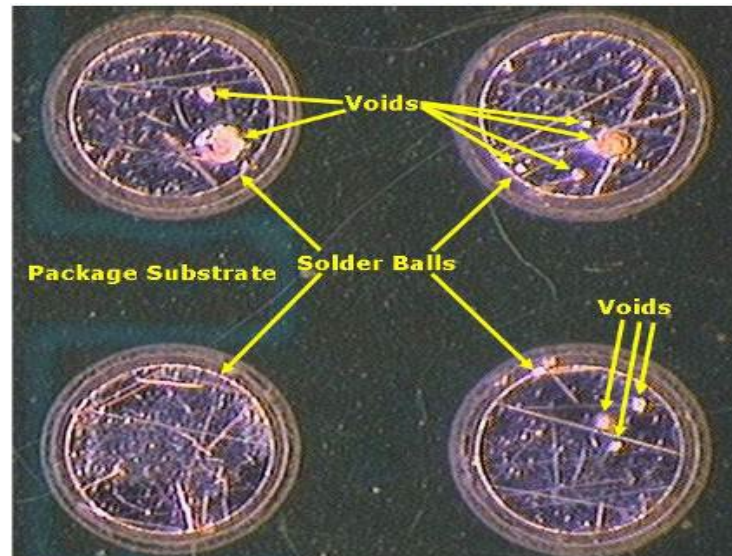
Figure 13 — Sequence of Grinding and Polishing Steps for Cross-Sectioning a BGA Package in the X-Y Plane

A photograph of the actual potted, ground and polished sample is shown in Figure 14 (a) and Figure 14 (b). This figure also includes a higher magnification photo with some voids visible within the cross-sectioned BGA balls.

6.3.5 Cross Section (cont'd)



(a)



(b)

Figure 14 — Cross-Section Views at Two Magnifications, Illustrating Voids in the BGA Balls.

This method works well with solder balls that have one or two large voids that are located in the center or near the package interface. With solder balls that have multiple voids dispersed throughout the ball it is difficult to find the maximum diameter of each void of interest. To find each void at its maximum diameter could take many grind and polishes.

- 2) Spatial void distributions within the package drive the need for iterative cross-sectioning of the sample.

6.3.5 Cross Section (cont'd)

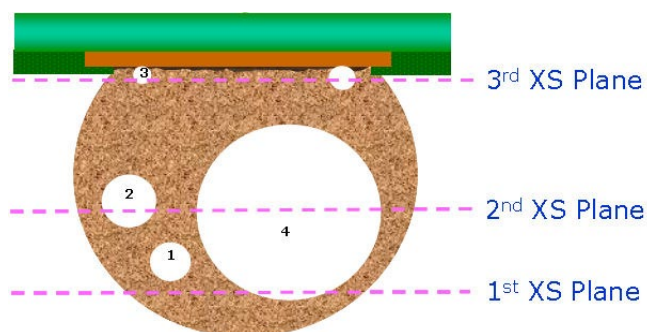


Figure 15 — X-Y Plane Diagram Showing the Location of Three Cross-Section Planes

In Figure 15, which contains an X-Z plane diagram of a cross-sectioned BGA ball, void #1 could be totally missed between grinds and polishing. There could also be issues with not measuring the true maximum diameter of the void as void #2 and void #3 are not at their maximum diameter. This is easy to do with smaller voids. Void #4 is at its maximum diameter and is much easier to reach because it is a large void. Larger voids allow for a bigger margin in finding the maximum diameter.

- 3) Another disadvantage to this method is the limited ability to compensate for package warpage. This issue is illustrated in Figure 16 and Figure 17.



Figure 16 — Diagram of a Warped BGA Package

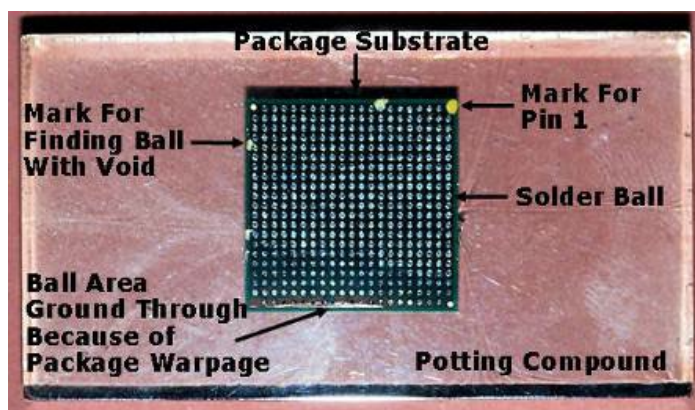


Figure 17 — Photo of the Actual Potted Package Showing Warpage

6.3.5 Cross Section (cont'd)

Packages that are warped are extremely hard to horizontally grind and polish evenly. The edge balls can be over half ground before the center balls are even a quarter of the way ground. If voids need to be measured in both the center and corners of the package then many multiple grind and polish iterations will need to be done. Figure 18 and Figure 19 show more views of warped BGA packages which illustrate the difficulty of obtaining void sizes in a single X-Y plane.

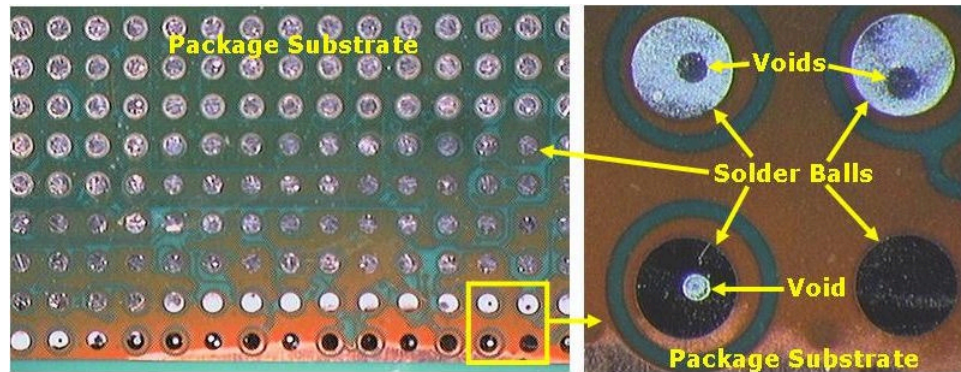


Figure 18 — Higher Magnification Views of Package Warpage Effects on Horizontal Grinding and Polishing Near the Package Edge.

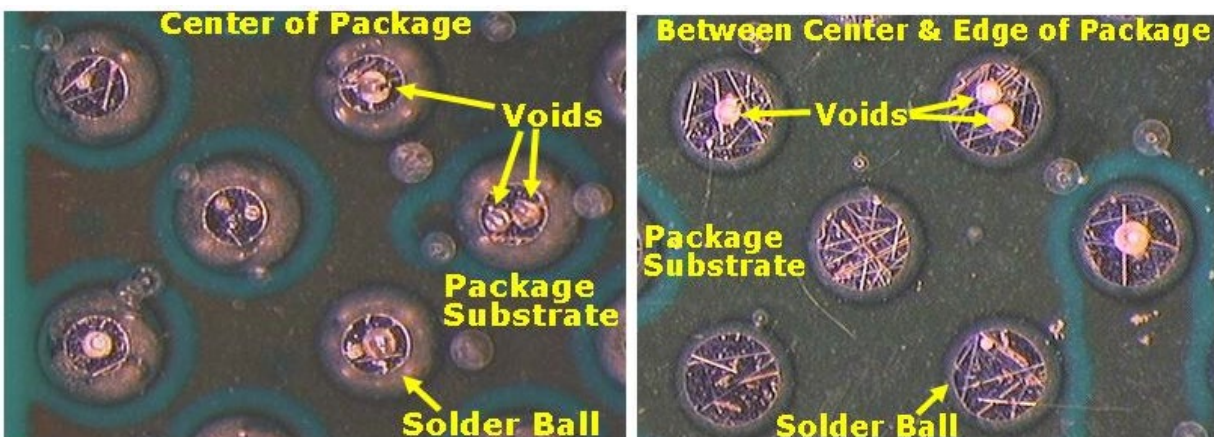


Figure 19 — Two Photos Illustrating Effects of Package Warpage on Horizontal Grinding and Polishing Across the Package

6.4 BGA Void Characterization Through Post BGA Ball Shear Pad Fracture Surface Inspection

If a BGA void exists in the failure plane of a BGA ball shear test, it may result in a characteristic circular feature at the pad fracture surface as shown in the images in Figure 20. The presence of voiding is more clearly discernible if the failure surface is indicative of a brittle failure. Characterization of voiding through fracture pad surface inspection is solely qualitative, as the void size and shape may be affected by the shear loading. It is also not possible to determine if the failure interface is at the maximum diameter of the void. Inspection post BGA ball shear can be used as an added BGA void monitor. If voiding is seen, further characterization is required, using the X-ray methods described by this document, for quantitative analysis.

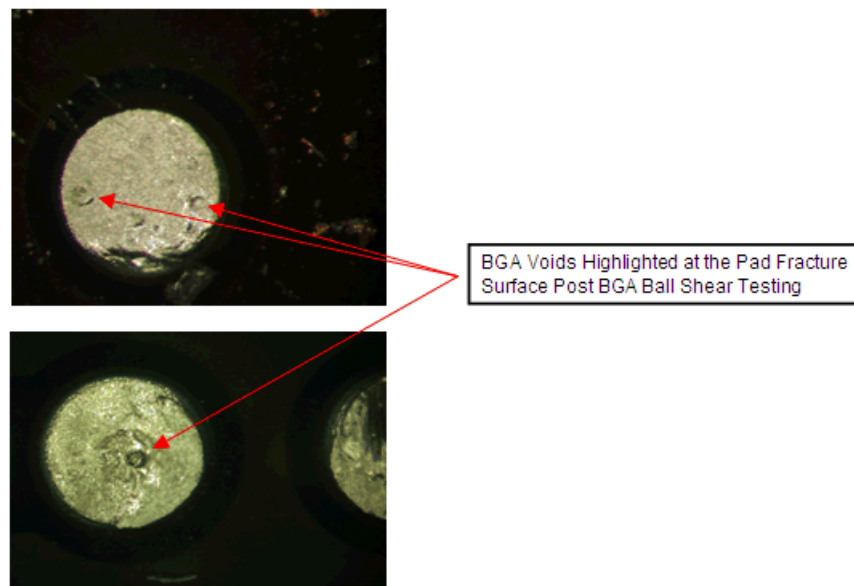


Figure 20 — Images of the Fracture Surface of a BGA Pad After a Ball Shear Test

7 Preferred Solder Void Metric

The metric chosen for quantitative determination of voids content in a solder ball is the cumulative % area of voids in the 2D X-ray image of a solder ball. This metric is consistent with IPC J-STD-001D and IPC-A-610 that list guidelines for post-SMT cumulative % area in the X-ray image area.

However, a detailed explanation of how this calculation is carried out is not contained within those documents. This has resulted in many instances within the industry of the metric being misunderstood and the cumulative % void area being miscalculated.

7 Preferred Solder Void Metric (cont'd)

For instance, the % area calculation is based on the ball area as seen in the X-ray Image. Some calculations have been based on using the BGA substrate or printed circuit board land area as the basis for the % calculation, instead of the ball outline area in the X-ray Image. The ball's outline is typically larger than the BGA or PCB land and as a result the cumulative % void area would be grossly over-estimated by using the land areas as opposed to the ball areas in the calculation.

The cumulative % void area within a solder ball X-ray image therefore needs further description and clear explanation. It is explained within IPC-7095B, *Design and Assembly Process Implementation for BGAs*. This is again described in more detail Figure 21.

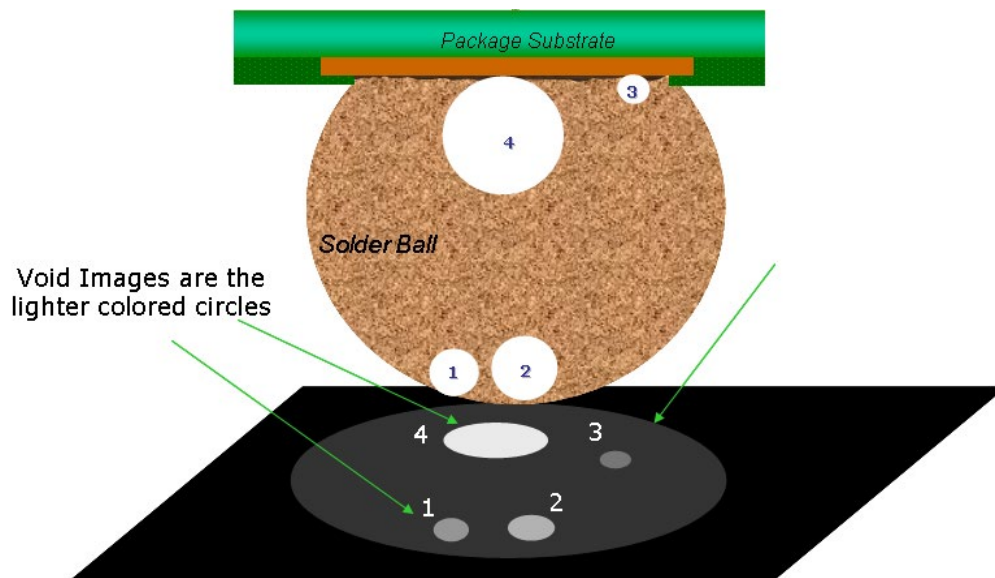


Figure 21 — Diagram Describing Cumulative % Void Area Computation Within 2-D Transmission X-Ray Image of a Solder Ball Containing Voids

The cumulative % void area of multiple voids in the X-ray image is calculated by first summing the area of each void in the ball and dividing this number by the area of the ball. This is the applicable equation for making this calculation.

$$\text{Cumulative \% Void Area in the Ball} = \frac{(\text{Area of Void 1} + \text{Area of Void 2} + \text{Area of Void 3} + \text{Area of Void 4}) * 100}{\text{Area of Solder Ball}}$$

One key point to stress here is that the measurement for void area is done with the 2-D X-ray image. Not all voids actually present in the ball may be visible in the X-ray image. A void could be so small as to not be visible in the X-ray image, either to the naked eye or to a software algorithm that identifies voids based on pixel gray scales.

7 Preferred Solder Void Metric (cont'd)

Some small voids could be obscured by larger voids in the top down plane as seen by the X-rays. Figure 22 illustrates some examples of this possibility.

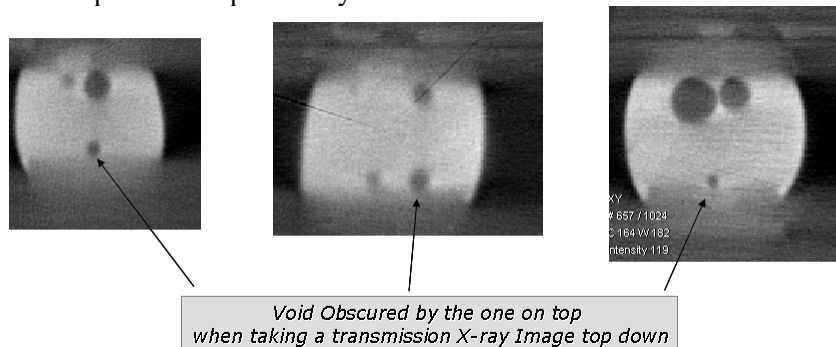


Figure 22 — X-Z Plane Slices of 3-D CT X-Ray Images Illustrating Small Voids Obscured by Larger Voids Located in the Same Top Down Plane Projected in 2-D Transmission X-Ray Images

Another possibility is the overlap of two or more voids in the top-down plane as seen by the 2-D transmission X-ray. This is shown in Figure 23. The three voids in this figure are not separated and hence the area occupied by the lighter void region will be less than that of the areas of the three voids combined, if they were distinctly apart in the X-ray image. However, though there will be some underestimation of the void areas from this image, it is still acceptable from the guideline standpoint since the void area in the image is what is the criterion and not the void area of the actual voids present in the ball.

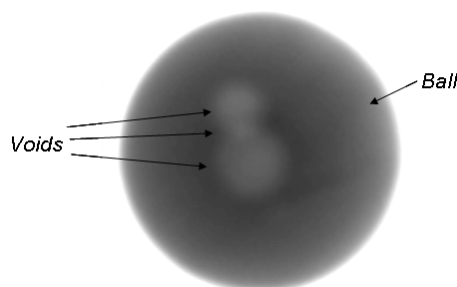


Figure 23 — 2-D Transmission X-ray Image of a Solder Ball with Three Overlapping Voids

NOTE Refer to Annex A for numerical examples of the solder void computation.

One major drawback for 2-D transmission X-ray metrologies has been the inability for automated software-driven algorithms to detect and measure voids of small diameters (<60 microns). An alternative proposed to overcome this shortcoming of the 2-D transmission X-ray metrology is to measure the void area of the *largest* void in a solder ball X-ray image, instead of *all* the voids detected. However, this approach has issues of its own. Table 2 list the pros and cons of the cumulative void % area for *all* voids vs. for the *largest* void in the solder ball X-ray image.

7 Preferred Solder Void Metric (cont'd)

Table 2 — Pros and Cons of the Cumulative Void % Area for *all* Voids vs. for the *largest* Void in the Solder Ball X-Ray Image

Void Calculation and Criteria	Pros	Cons
Cumulative Void Area % of ALL Voids	Covers all voids in a ball	Metrology limitation in Small Void Area measurement for Automated 2D Transmission X-ray Systems
	Consistent with J-STD-001/610-D Post SMT Spec	More time consuming if Manual Measurement Metrology is Employed Perception is that its aggressive from Supplier Point of View
	Covers Worst Case Scenario from Customer Point of view	Calculation has been mis-understood and wrongly applied in the industry
LARGEST Void Area %	Less Time Consuming if Manual Measurement Metrology is Employed	Not consistent with J-STD-001 / 610-D Post SMT Industry Spec
	Void Size Measurement Limitations with Automated 2D Transmission X-ray Systems are significantly lower	Does NOT cover worse case scenario from Customer Point of View;
	Simple to Understand and Implement	Two instances where this calculation would grossly underestimate actual void presence in the BGA Ball are when Ball has two large voids of similar size or One large void with multiple small voids (See Annex A)
	Perception is that its too lenient from Supplier Point of View	

8 Preferred Solder Void Metrology

In selecting the solder void detection metrology, considerations should be taken on the relative accuracy, precision, equipment availability, repeatability and cost, and throughput.

For majority of applications, 2-D X-ray transmission tool is an appropriate metrology especially for detection of macrovoids where good correlation to 3-D X-ray was observed in terms of solder void computational accuracy. Annex B provides results of statistical studies between 2-D and 3-D X-ray tools from round robin experiments (package and digital images).

9 Sampling Plan

Table 3 provides a set of sampling guidelines for solder void characterization based on the traditional AQL approach for solder ball level with $\alpha = 0.05$. A minimum of 3 units is recommended. Corrective measures would be considered if the number of balls with voids above cumulative void % guidance exceeded the acceptance number (c).

However, other AQL targets and sampling strategies may be considered according to the purpose of the data collection (process development, process transfer, process monitoring, product development or control, etc.). For instance, if significant data was collected and a stable baseline is established, employment of variable-data type approach could be considered (e.g., statistical mean and variance).

Table 3 — Sample Sizes for Voids Measurement in BGA Solder Balls for Various Acceptance Numbers and AQL

Acceptance Number	AQL		
	1%	2.5%	4%
C=0	5	*	*
C=1	35	14	9
C=2	82	33	21
C=3	137	55	34
C=4	198	79	50
* No sampling plan available to meet the conditions.			
NOTE Refer to JESD47 for other sampling alternatives.			

10 Void Guideline

Recent studies on pre to post SMT void growth have established an upper limit of 10%. Hence, a pre-SMT guideline of <15% cumulative voiding is recommended in order to meet post-SMT guidelines noted in other standards (e.g. IPC-J-STD-001E and IPC-A-610E). These studies are consistent with previous surveys.

NOTE Refer to Annex C for results of recent studies on solder void growth characterization.

Companies may consider other options for internal solder void guidelines based on process stability, capability, quality requirements, and reliability performance. Some packages may be more susceptible to solder void formation, and thus require more restrictive sampling and/or voiding limits.

Annex A Calculation of Cumulative % Void Area Within Solder Balls (1 or Multiple Voids in the X-Ray Image)

The metric chosen for quantitative determination of voids content in a solder ball is the cumulative % area of voids in the X-ray image of a solder ball. As noted in Section 8, this calculation has been used incorrectly in the industry for BGA solder joints and needs further description and clear explanation.

Hence, how to calculate the cumulative % area of voids in an X-ray image is explicitly shown in Figure 24 for three examples. These three examples are for 1, 3 and 5 voids in the solder ball X-ray image. This figure is similar to one that appears in the IPC-7095B document entitled *Design and Assembly Process Implementation for BGAs*.

First, the ball area is calculated by measurement of the diameter of the ball outline in the image after some adjustment in gray scaling. Then, each void area is calculated by measuring the diameter of the visible void outline in the image. Next, the void areas are summed. Finally, this number is multiplied by 100 and divided by the ball area to determine the cumulative % void area.

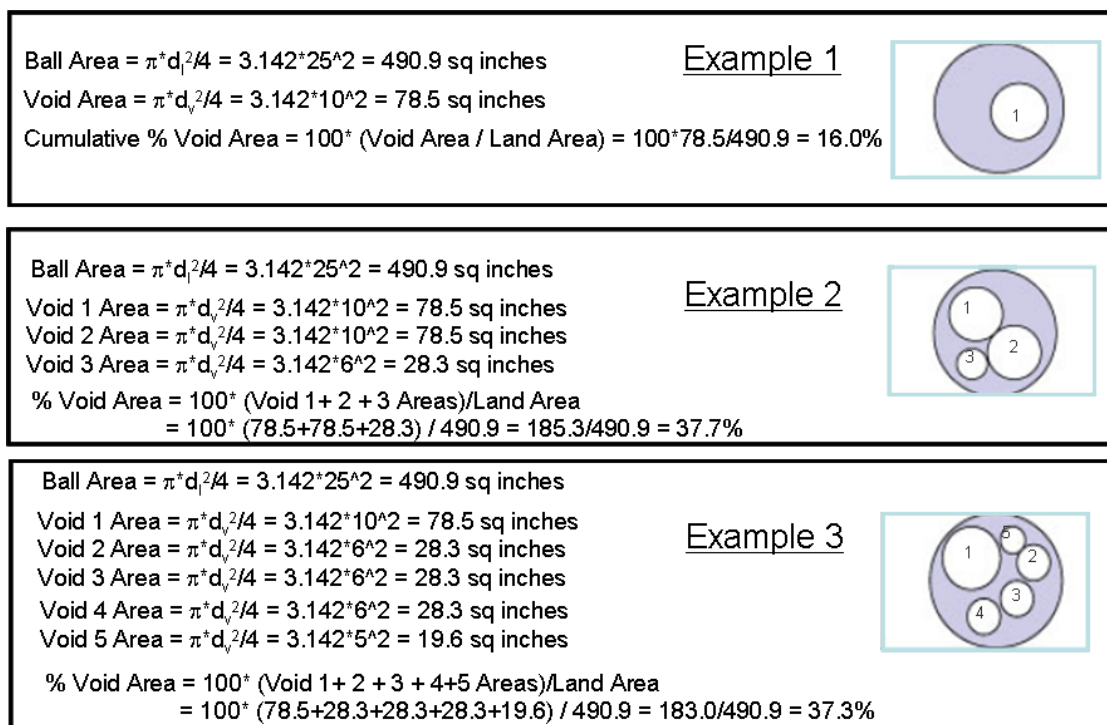


Figure 24 — Examples of Cumulative % Void Area Calculation for Solder Balls Containing 1, 3, and 5 Voids in the Solder Ball X-Ray Image.

A.1 Comparison of Cumulative vs. % Void Area for Largest Void for Three Examples of Voids in Solder Balls

As explained in clause 8, automated 2-D transmission X-ray metrologies are unable to detect and measure voids of small diameters (<60 microns). One alternative proposed to overcome this shortcoming of the 2-D Transmission X-ray Metrology is to measure the void area of the *largest* void in a solder ball X-ray image, instead of *all* the voids detected.

Table 4 compares the cumulative % void area for all voids with the % Void Area for the Largest Void in the three examples shown in Figure 24. It is apparent from this table that if there is only one large void in the solder ball, the two metrics – cumulative vs. largest – are not significantly different. But, if the solder ball contains two or more large voids or one large void with multiple small voids, then there is a significant difference between these two metrics, with the % Void Area for Largest Void *grossly underestimating* the void area in the solder ball X-ray image.

Table 4 — Comparison of the Cumulative % Void Area for all Voids with the % Void Area for the Largest Void in the Three Examples Shown in Figure 24

Example #	Cumulative % Void Area for All Voids	% Void Area for Largest Voids	Difference between Cumulative vs. Largest Void	Description of Voids Distribution in Solder Ball
1	16	16	0	One Large Void
2	37.7	16	21.7	Two Large Voids
3	37.3	16	21.3	One Large Void with multiple small voids

Annex B 2-D X-Ray Void Detection to 3-D Correlation X-ray Correlation Study

To better understand 2-D X-ray capability, site-to-site correlation, and validate metrology limitations, two round robin studies were developed and executed by a JEDEC JC-14.1 Task Group.

For round robin 1, two types of FCBGA packages ('P' and 'D') were sent to companies participating in the Task Group. Each company would compute cumulative void % on specific balls before sending those packages to the next participant. In round robin 1, there were 4 participants (Freescale, Intel, IBM, and Texas Instrument). Each site measured a total of 6 packages (3 per type) and more than 30 balls per package.

For round robin 2, digital images from 2-D X-ray of two types of packages ('P' and 'D') were taken by a single site; specific voids were demarked from each digital image to eliminate identification errors. Images were then sent to various Task Group participants to individually compute cumulative void %. Later, images were also sent to an independent institution (Hong Kong University) for verification. For round robin 2, images were taken from a total of 6 packages (3 per type) with 11 balls selected for each package.

For both round robin exercises, voids were also computed using 3-D CT X-ray to evaluate metrology capability and overall accuracy. Also, criteria for metrology matching and correlation were consistently maintained. Table 5 illustrates the criteria.

Table 5 — Criteria and Requirements for Two BGA Void Metrologies to Match

Criterion	Requirement
Correlation Coefficient (R^2)	>0.750
Slope	Statistically Equivalent to 1
Bias	Not Significant

Table 6 — Round Robin 1 Results

		2-D results Mean/sigma	3-D results Correlation Mean/sigma	Acceptable
Intel	Pkg P	10.73/2.95	0.44/11.29/3.01	No
	Pkg D	4.12/2.45	0.84/5.74/2.97	No
Freescale	Pkg P	12.65/3.16	0.79/11.29/3.01	Yes
	Pkg D	7.16/3.38	0.86/5.74/2.97	No
IBM	Pkg P	9.47/2.53	0.97/11.29/3.01	No
	Pkg D	7.95/4.08	0.82/5.74/2.97	No
Texas Instrument	Pkg P	10.25/3.48	0.60/11.29/3.01	No
	Pkg D	4.83/2.75	0.90/5.74/2.97	No

Annex B 2-D X-Ray Void Detection to 3-D Correlation X-Ray Correlation Study (cont'd)

Results from Round Robin 1 are illustrated in Figure 25. Most R^2 for package 'D' (green marks) are acceptable ($R^2 > 0.75$). However, package 'P' (red dots) did not meet matching criteria for correlation coefficient.

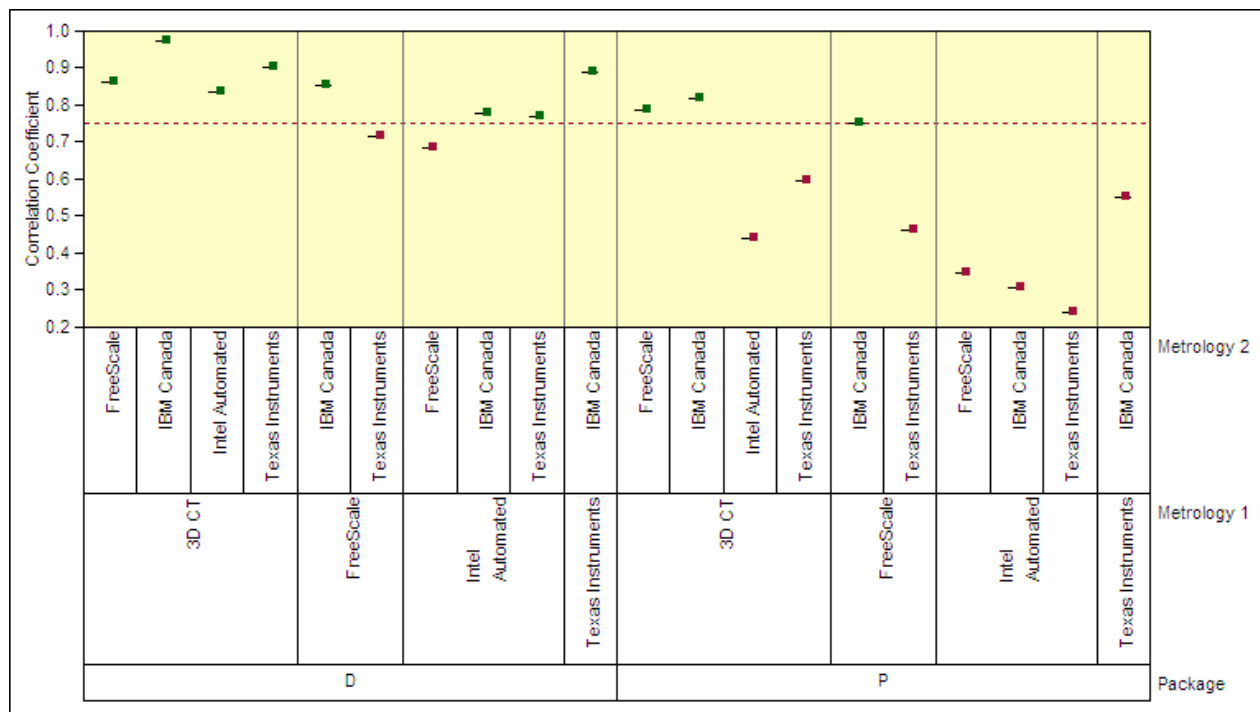


Figure 25 — Variability Chart of the Correlation Coefficient for Various Pairs of Metrologies for Round Robin 1

A closer examination on the void signature for package 'D' and 'P' reveals using 3-D CT X-ray indicated predominance of voids of small diameter (<60 microns) in package 'P.' As discussed before, 2-D X-ray is less consistent in capture these types of voids. Additionally, small voids were also attributed to misidentification of voids among different sites. Figure 26 indicates the differing void sizes for packages 'D' and 'P.'

Annex B 2-D X-Ray Void Detection to 3-D Correlation X-Ray Correlation Study (cont'd)

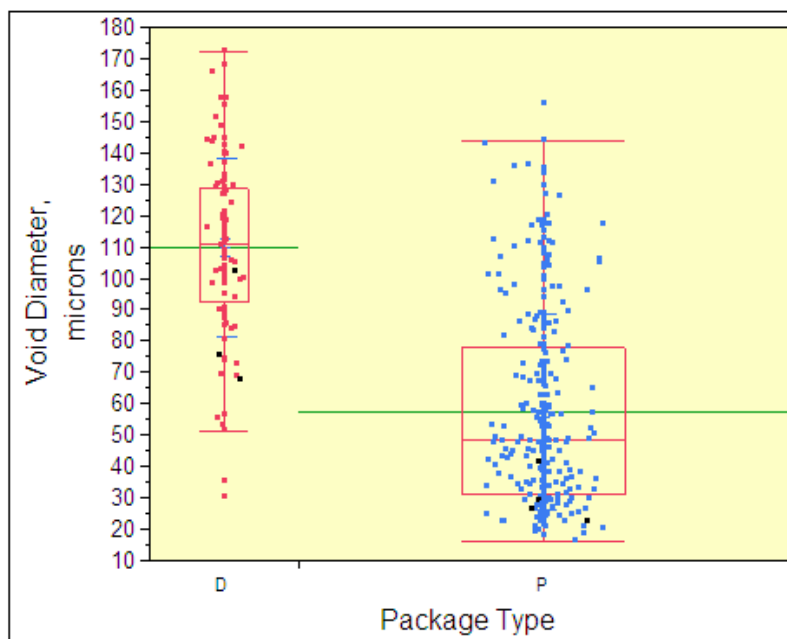


Figure 26 — Box Plots of Void Diameters in Microns Measured within the BGA Balls of Packages ‘D’ and ‘P’ Using 3-D CT X-ray Metrology

Table 7 — Round Robin 2 Results

Metrology	Package Type	2-D results mean/sigma	3-D results Correlation coefficient/ mean/sigma	Acceptable
Intel Automated	Pkg P	10.27/4.04	0.57/10.62/3.37	No
	Pkg D	4.99/2.94	0.88/6.69/3.44	Yes
Intel Manual	Pkg P	11.12/3.47	0.88/10.62/3.37	Yes
	Pkg D	7.57/3.98	0.97/6.69/3.44	Yes
Freescale	Pkg P	12.81/3.38	0.83/10.62/3.37	Yes
	Pkg D	7.41/3.80	0.96/6.69/3.44	Yes
IBM	Pkg P	9.49/2.87	0.90/10.62/3.37	Yes
	Pkg D	5.61/3.02	0.96/6.69/3.44	Yes
Texas Instrument	Pkg P	10.09/3.97	0.68/10.62/3.37	No
	Pkg D	5.82/3.46	0.92/6.69/3.44	Yes
Oracle	Pkg P	12.46/3.2	0.72/10.62/3.37	No
	Pkg D	8.51/4.27	0.97/6.69/3.44	Yes
Hong Kong University	Pkg P	11.40 /3.41	0.88/10.62/3.37	Yes
	Pkg D	6.64/3.44	0.96/6.69/3.44	Yes
ST Micro	Pkg P	12.18/3.33	0.83/10.62/3.37	Yes
	Pkg D	9.23/4.42	0.92/6.69/3.44	Yes

Annex B 2-D X-Ray Void Detection to 3-D Correlation X-Ray Correlation Study (cont'd)

As mentioned before, to eliminate identification errors, digital images were sent to each round robin participant. Figure 27 is an example of one digital image.

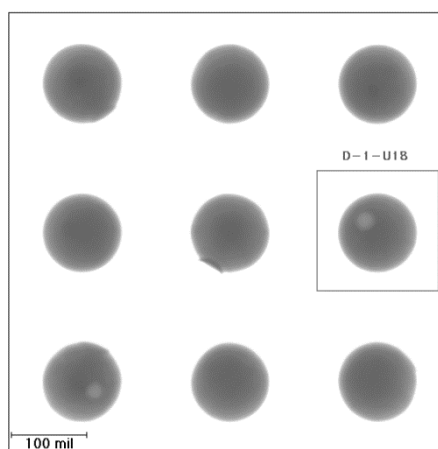


Figure 27 — Digital Image of Solder Ball with Marked Location for Solder Void Computation

Results from Round Robin 2 are illustrated in Fig 28. With each participant computing solder voids from digital images, expected coefficient of correlation was easily met for package ‘D’ ($R^2 > 0.75$). For package ‘P,’ results were much improved from Round Robin 1 with two marginal (R^2 at 0.70), and one misaligned datapoint with use of automated solder void computation algorithm. These results reinforce the need to understand tool variations, and importance to follow inspection guideline as well as account for metrology limitations (small voids and software algorithm). Considering these aspects, 2-D X-ray does provide accurate solder void measurements as observed in the correlation to 3-D X-ray.

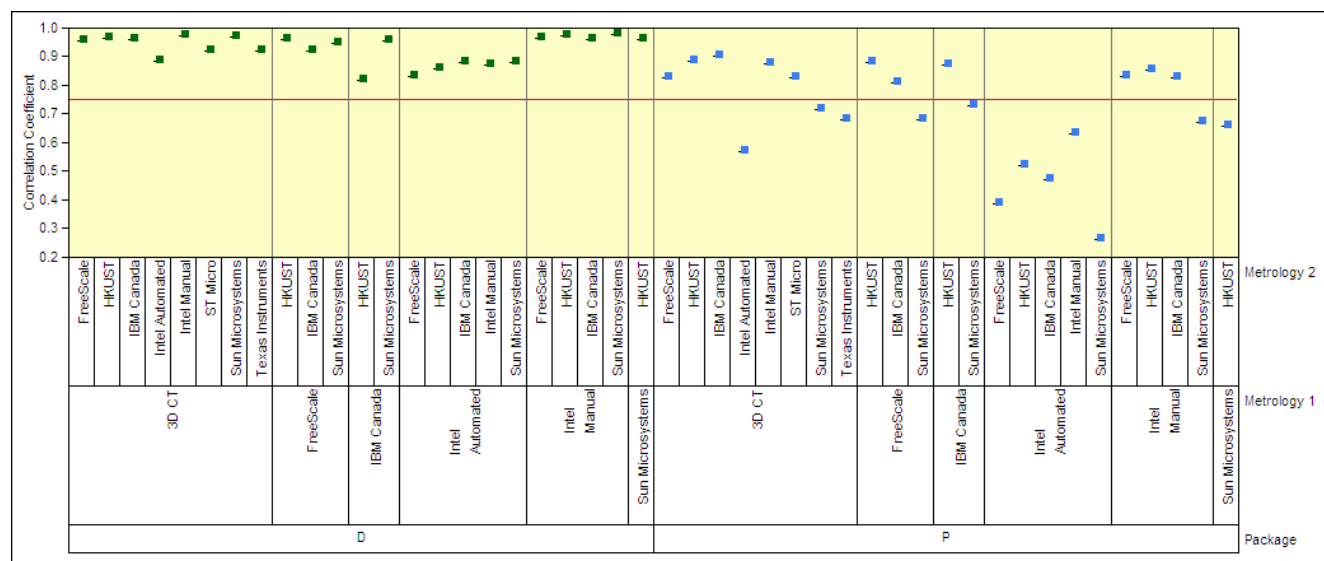


Figure 28 — Variability Chart of the Correlation Coefficient for Various Pairs of Metrologies for Round Robin 2

Annex C Solder Void Growth Characterization Results

As part of efforts to determine an appropriate pre-SMT tolerance limit for cumulative void % in the solder ball that would be aligned to existing IPC documents for post-SMT acceptability, JEDEC JC-14.1 Task Group developed three studies to characterize solder void growth during SMT process.

Figure 29 graphically depicts the objective of these studies.

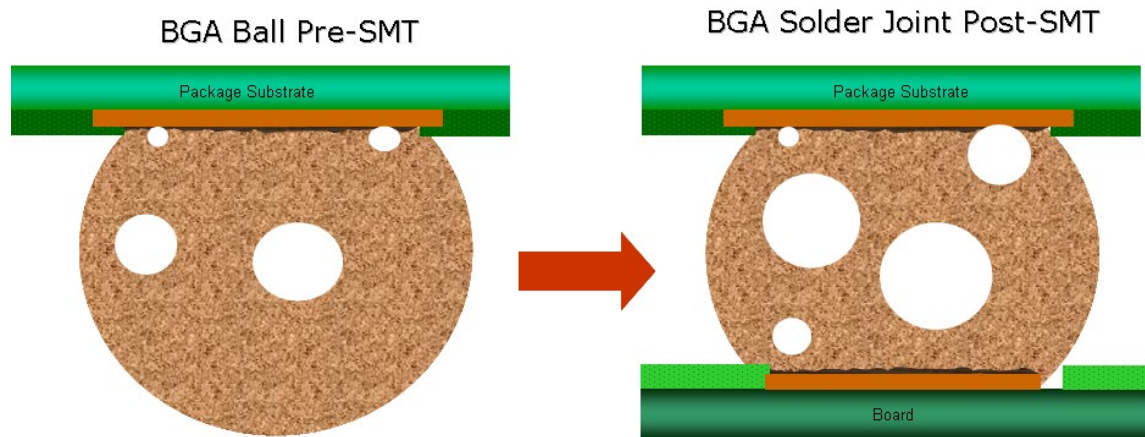


Figure 29 — Illustration of the Solder Ball Void Change During SMT Soldering Process - Package to Board

During SMT soldering process, these potential scenarios (growth or reduction) can occur:

- Macro Void Generation: large voids that are formed by: a) trapped water vapor or b) effluents from solder paste vehicle.
- Macro Void Coalescence: two or more macro voids in close proximity that coalesce together to form larger voids.
- Planar Microvoid Generation: small voids that may be generated from Cu caves under printed circuit board surface finish (example Immersion Silver) of board lands.
- Microvia-in-Lands Voids: voids that are formed from trapped air located in the microvia in the board lands.
- Macro Void Escape: Macro voids close to the surface of the solder ball escape to the surrounding air when the solder is molten.

C.1 Solder Void Growth Characterization - Study 1

In Study 1, two different flip chip BGAs (package 'C' and 'R') were utilized. Cumulative solder void % was computed for each solder ball from 3-D CT x-ray prior and post-SMT processing. For package 'C', a total of 320 solder balls over 20 packages which were selected from 9 different ball attach lots. For package 'R', 384 solder balls over 24 packages selected from 12 different lots.

Table 8 — Results of the Solder Void Growth – Study 1

Cumulative % Void Area	Pre-SMT Mean/Sigma	Post-SMT Mean/Sigma	Solder Void Change (95% confidence)
Package 'C'	0.5 / 1.3	2.8 / 2.3	+2.3
Package 'R'	2.6 / 1.8	5.9 / 3.5	+3.3

Figure 30 displays the box plots for the Cumulative % Void Area growth during the SMT process for packages 'C' and 'R'.

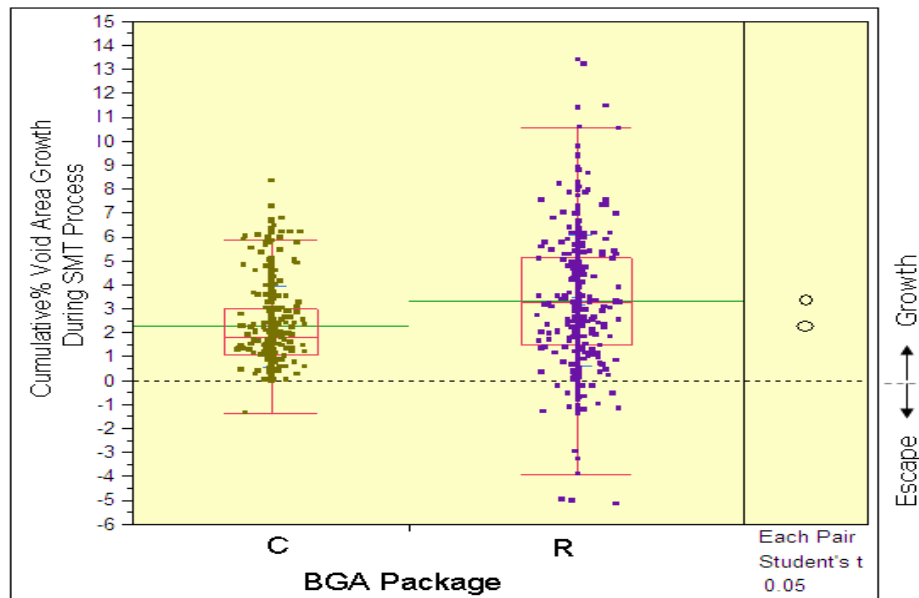


Figure 30 — Void Growth in Packages 'C' and 'R' During the SMT Soldering Process

Results from Study 1 reveals minimum solder void growth for both packages (package 'C' at 2.3% and package 'R' at 3.3%). The maximum void growth observed were 8.3% and 13.4% respectively. Considering a 95% confidence limit, the upper limit is approximately 10% cumulative void.

Further analysis on solder void behavior from Study 1 is illustrated in Table 9. It indicated a positive trend with increase in the number of voids as well as cumulative % void area.

C.1 Solder Void Growth Characterization - Study 1 (cont'd)

Table 9 — % of Solder Balls that had no Voids, an Increase and Reduction in Cumulative % Void Area for Two BGA Packages

Cumulative Void %	Package 'C'	Package 'R'
% of units with no voids prior or after SMT	2.8%	0.0%
% of units w/ void increase during SMT	95.6%	91.9%
% of units w/ void reduction during SMT	1.2%	8.1%

Despite positive trend described in Table 9, there was a weak correlation (ball to ball) recorded in Study 1 ($R^2=0.38$). This weak correlation implies that the void magnitude in a BGA ball before soldering is not necessarily a strong contributor to the void magnitude after SMT reflow process.

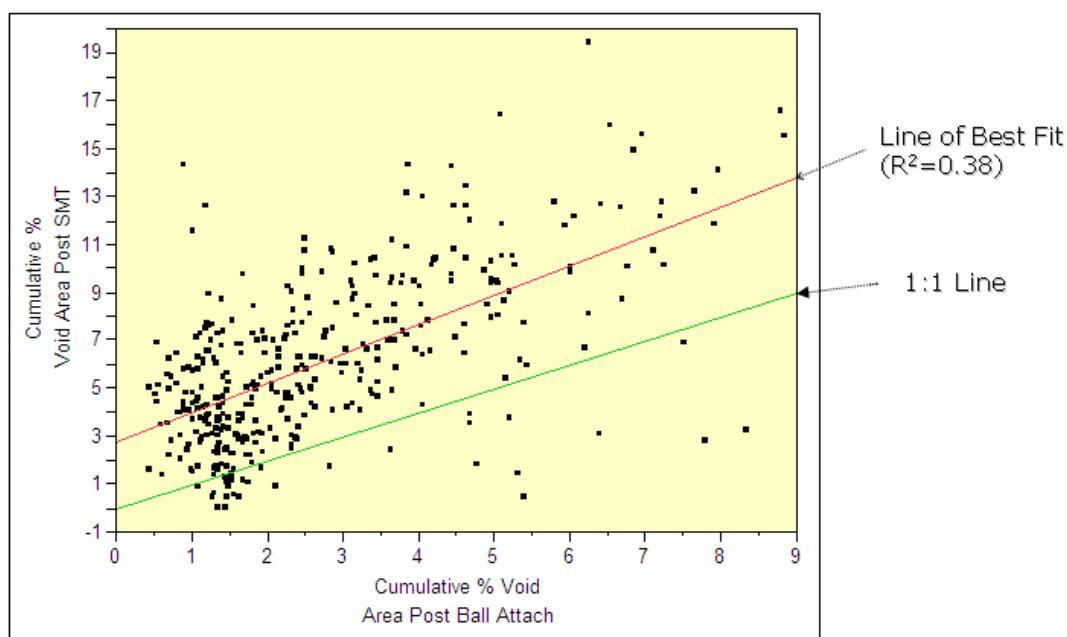


Figure 31 — Correlation on Cumulative % Void Area (Post Ball Attach to Post SMT) for Package 'R'

C.2 Solder Void Growth Characterization - Study 2

Study 2 was designed to assess robustness of <15% cumulative void tolerance guideline recommended in this document. This study was driven by Texas Instrument and Oracle, and implemented at Hong Kong University of Science and Technology (HKUST). Ceramic ball grid array (CBGA) packages from Texas Instrument, referred to package 'T', were used in this study.

C.2 Solder Void Growth Characterization - Study 2 (cont'd)

In order to generate voids near 15% cumulative void level, non-standard process was employed to the CBGA packages after standard ball attach process with subsequent reflow of solder balls in a reservoir of the same ball attach flux.

Cumulative % void values were measured in the same 30 solder balls pre and post SMT to determine void growth. Table 10 lists the mean and standard deviation (sigma) for both pre- and post-SMT. There was a mean 3.3 % cumulative void growth during the SMT process.

Table 10 — Results of the Solder Void Growth – Study 2

Cumulative % Void Area	Pre-SMT Mean/Sigma	Post-SMT Mean/Sigma	Solder Void Change (95% confidence)
Package 'T'	14.9 / 1.8	18.2 / 2.0	+3.3

Figure 32 compares the two box plots for Cumulative % Void Area for package R post ball attach (before SMT reflow) and Post SMT reflow soldering. As shown in Table 10, there is void growth occurring during the SMT process for this study. The maximum void growth measured was 6.2%. None of the post SMT solder joints exceeded the level specified in the industry standards for post SMT requirements of solder joints. This implies that void levels in the 12 to 18% cumulative voids prior to SMT reflow will still be able to meet the industry standard post SMT reflow requirement for the maximum for voids within BGA solder joints.

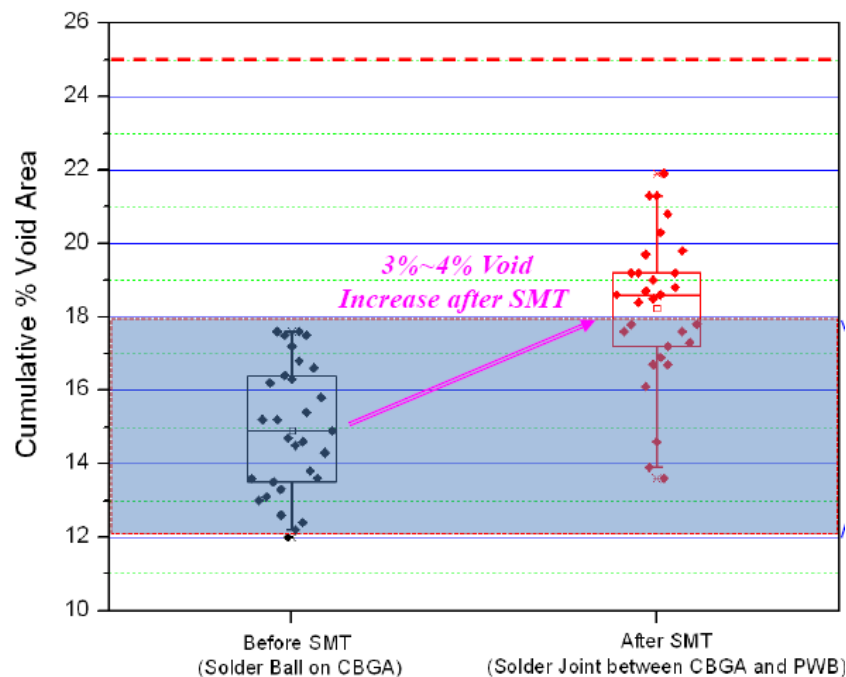


Figure 32 — Post Ball Attach and Post SMT Cumulative % Void Area Data for 30 balls of CBGA Package 'T' at HKUST

C.3 Solder Void Growth Characterization - Study 3

Void growth characterization study 3 shared similar objectives to Study 2 to determine overall robustness of proposed <15% cumulative void tolerance guideline, but under different ball attach processes and SMT manufacturing line.

Again, special skewed processes were utilized to generate voids near the 15% cumulative void areas during the ball attach process. 10 packages 'R' were selected from three different lots with different types of solder pastes and chemistries: a) No Clean, Halogenated, b) No Clean, Halogen-free, c) Water Soluble, and Halogen-free.

A total of 63 solder balls were measured for cumulative voids pre and post-SMT using 2-D transmission X-ray as recommended metrology. 3-D CT X-ray was also used to validate 2-D X-ray tool accuracy and aid once again in further evaluation of solder void transitional behavior. From the 63 selected solder balls, 16 balls were from 3 packages that had the no clean, halogenated ball attach paste, 16 were from 3 packages that had the no clean, halogen-free ball attach paste, and 31 were from water clean, halogen-free ball attach paste.

Results of Study 3 are shown in Figure 33. It is apparent that there is a decrease in the mean of the cumulative % Void Area during the SMT process in this study.

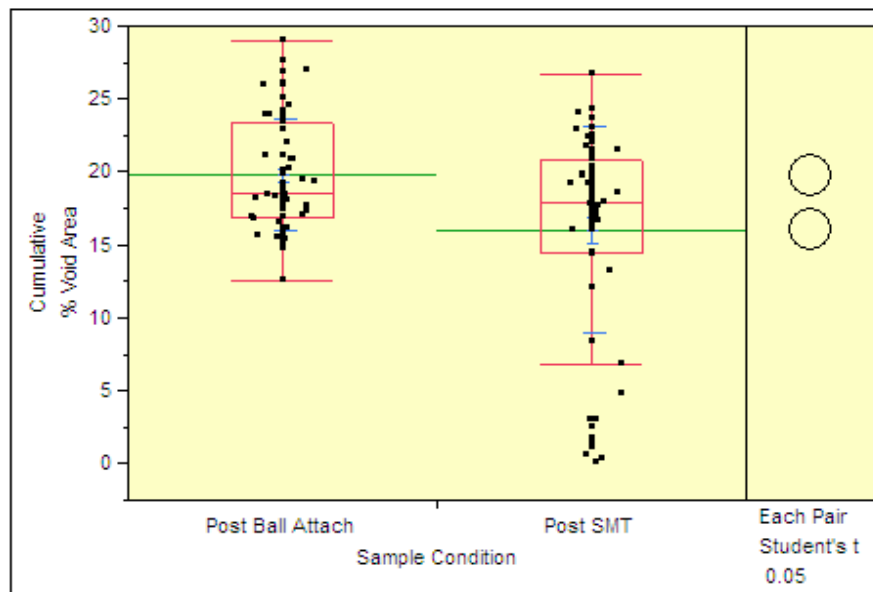


Figure 33 — Post Ball Attach and Post SMT Cumulative % Void Area Data for 63 Balls of BGA Package 'R'

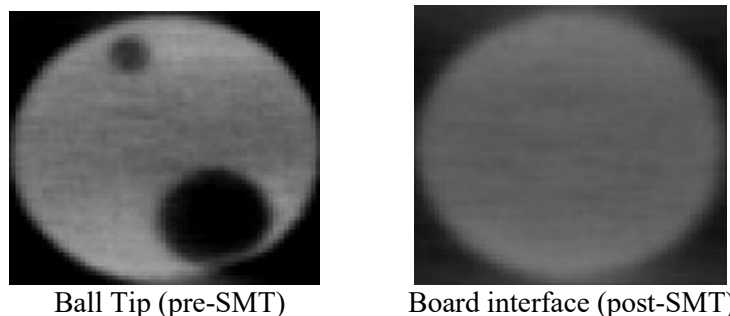
C.3 Solder Void Growth Characterization - Study 3 (cont'd)

Table 11 shows the mean and standard deviation (sigma) of the cumulative % void area pre-SMT and post-SMT for this study. There is a *decrease* of 3.7% in the cumulative % void area during the SMT process.

Table 11 — Results of the 15% Solder Void Growth – Study 3

Cumulative % Void Area	Pre-SMT Mean/Sigma	Post-SMT Mean/Sigma	Solder Void Change (95% confidence)
Package ‘R’	19.7/3.81	16.0/7.09	-3.7

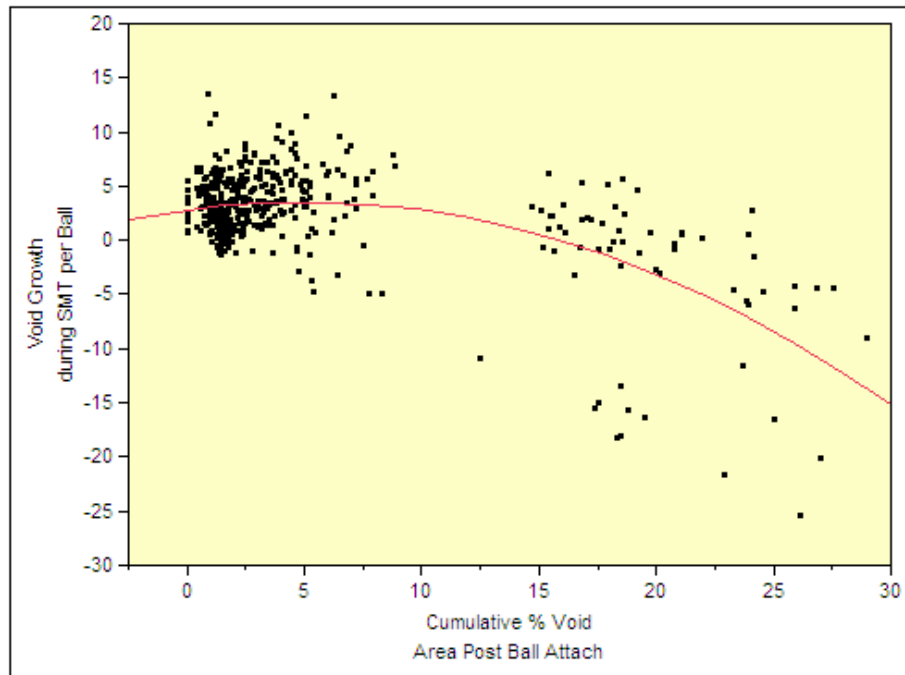
From these results, it is clear that solder voids do not necessarily increase from SMT reflow. Unlike Study 1 and Study 2, overall mean in Study 3 in fact decrease implying that larger voids may escape during SMT reflow process when the solder was molten. 3-D CT X-ray analysis reveal that larger voids located at the solder ball edge did in fact escape after SMT (Figure 34).



**Figure 34 — 3-D CT X-Ray of Solder Void Change from pre-SMT to post-SMT
with Larger Void Escape**

A summary of the solder void growth variation is seen in Figure 35. It shows void growth in Package ‘R’ solder balls during SMT reflow process. With the cumulative % void area in the solder balls before the SMT process. Significant scatter is observed, and the best fit curve shows that the maximum void growth during SMT occurs when the pre SMT void content in the solder ball is between 5 and 10% cumulative void area. AT higher void contents, post SMT, more voids escape from the ball than are formed during the SMT reflow soldering process.

C.3 Solder Void Growth Characterization - Study 3 (cont'd)



**Figure 35 — Variation in Package ‘R’ Void Growth during SMT Reflow Process
(post Ball Attach to post SMT)**

C.4 Justification of Proposed 15% Cumulative Void Area Guideline for BGA Balls Post Ball Attach

Three solder void growth characterization studies have shown that <15% cumulative % void area tolerance guideline is suitable to meet post-SMT industry expectation following J-STD-001E and IPC-A-610E. These studies interjected both package as well as process variability to evaluate robustness of the guideline. In addition, studies were designed to test the tolerance guideline with voids at or above 15% cumulative % void area. The overall result, despite inconsistent trends regarding solder void transitional behavior during SMT reflow, reveal that overall void growth measurements were all within <10% cumulative % void area; hence providing adequate margin to meet post-SMT target.

Annex D (Informative) Differences Between Revisions

Table 12 briefly describes the minor changes made in this standard, JESD217A compared to its predecessor, JESD217.01 (October 2016).

Table 12 — Differences Between JESD217A and Prior Versions

Clause:	Differences Between JESD217.01 and JESD217A:
Introduction	Use of ‘device’ to replace ‘component’ in alignment to JESD88.
2	Update of Pb Free in alignment with J-STD-020 and inclusive of Low Temperature Solder .
3	Update to J-STD-609 title.
	Differences Between JESD217 and JESD217.01:
7	1 st para.: Removal of explicit guidelines listed in IPC documents (% void area); last 2 sentences modified.
10	1 st para.: Removal of explicit guidelines listed in IPC documents (% void area); second sentence modified.
C.2	4 th para.: Update on the % area tolerance for the illustration reflecting IPC document for post-SMT void guideline; removed 25% in 2 places.

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Standard Improvement Form**JEDEC****JESD217A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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-
1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

-
2. Recommendations for correction:

-
3. Other suggestions for document improvement:

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